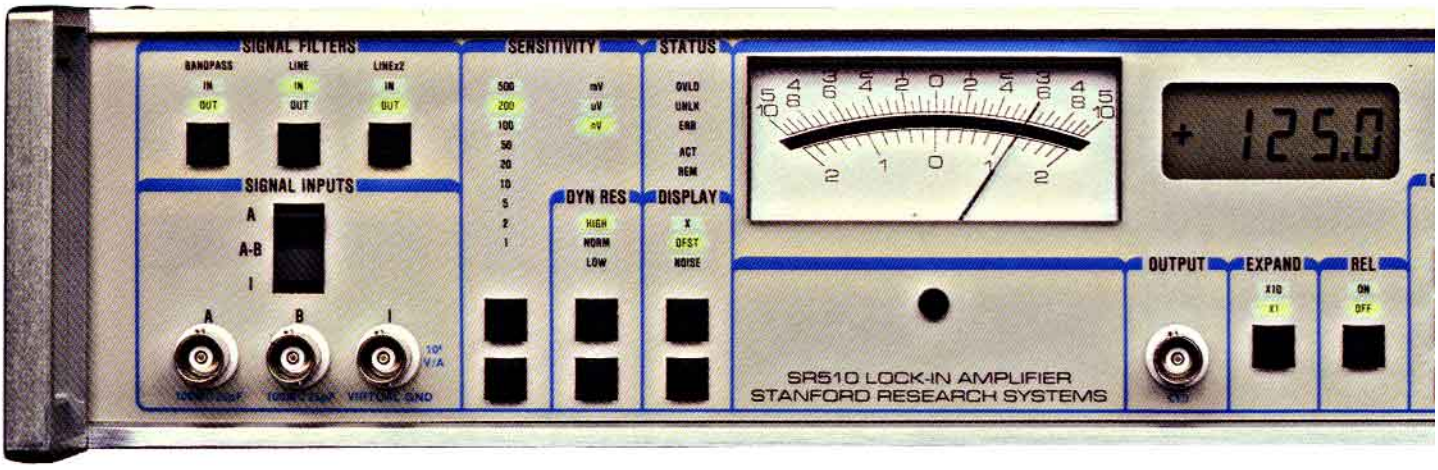
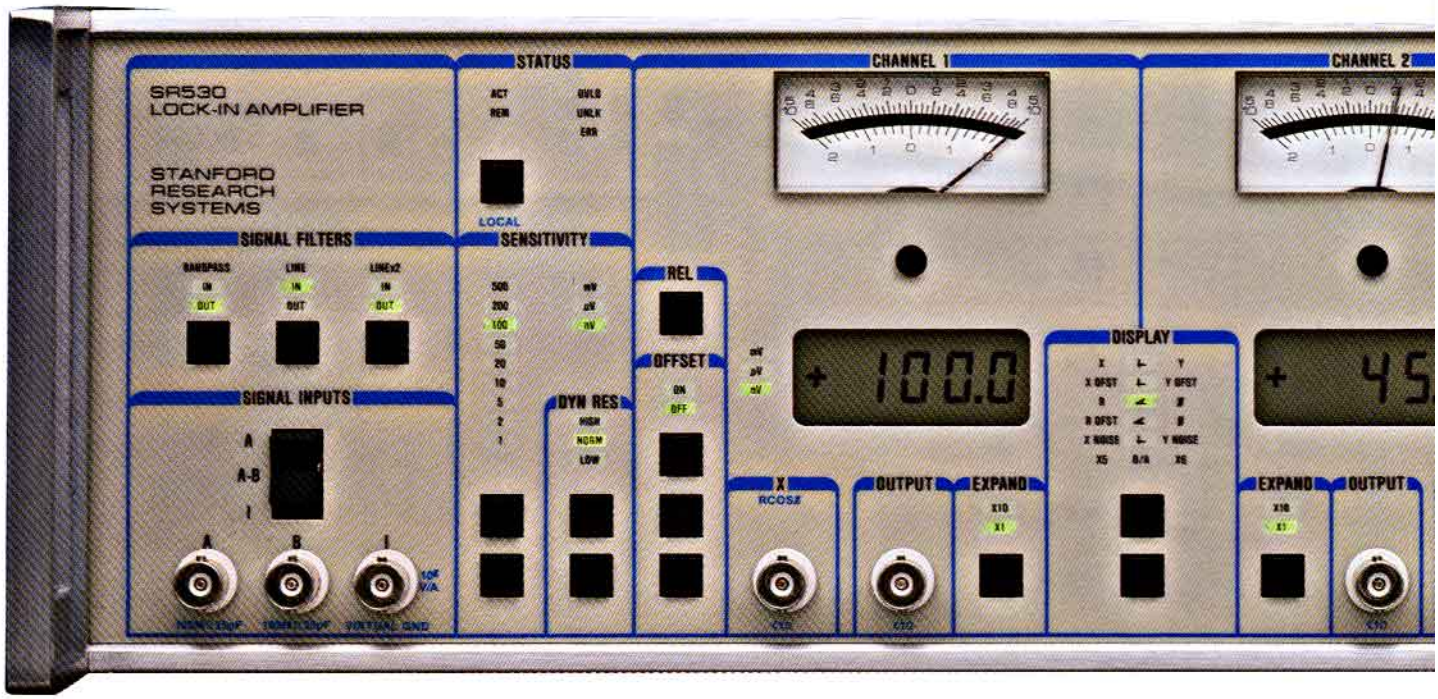
LOCK-IN AMPLIFIERS

Stanford Research Systems, Inc.

SR510 SINGLE PHASE LOCK-IN—



SR530 TWO PHASE LOCK-IN—



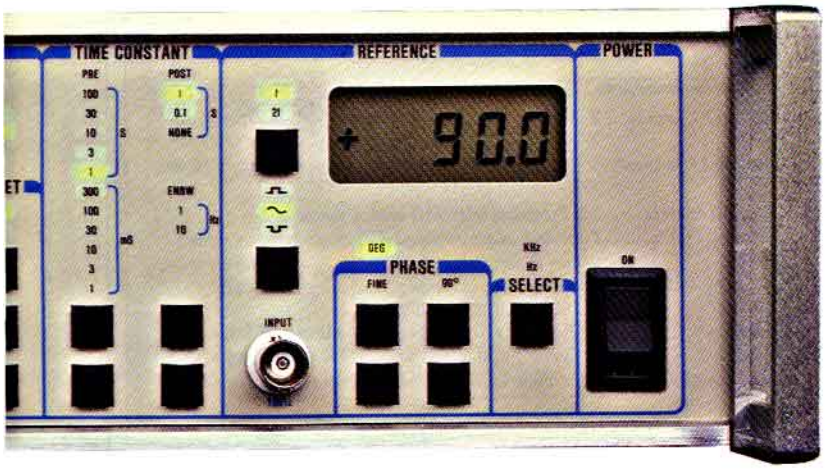
TWO PHASE AND SINGLE PHASE

Two new lock-in amplifiers from Stanford Research Systems represent the latest in instrument design and performance for ac signal recovery. Both units have many features that are either unavailable or are costly options on other lock-ins. The SR530 Two Phase Lock-in provides simultaneous measurement of Vector Magnitude and Signal Phase. The SR510 Single Phase Lock-in measures the amplitude of your signal at a specified phase.

POWERFUL PERFORMANCE

Over the 1 Hz to 100 kHz operating range, both lock-ins will measure signals down to 10 nV full scale while rejecting interfering signals up to 100,000 times larger. Maximum flexibility to optimize your experiment is provided by an auto-tracking bandpass filter, two line notch filters, and three input modes: single-ended voltage, true-differential voltage, and current input.

MANCE AND RELIABILITY



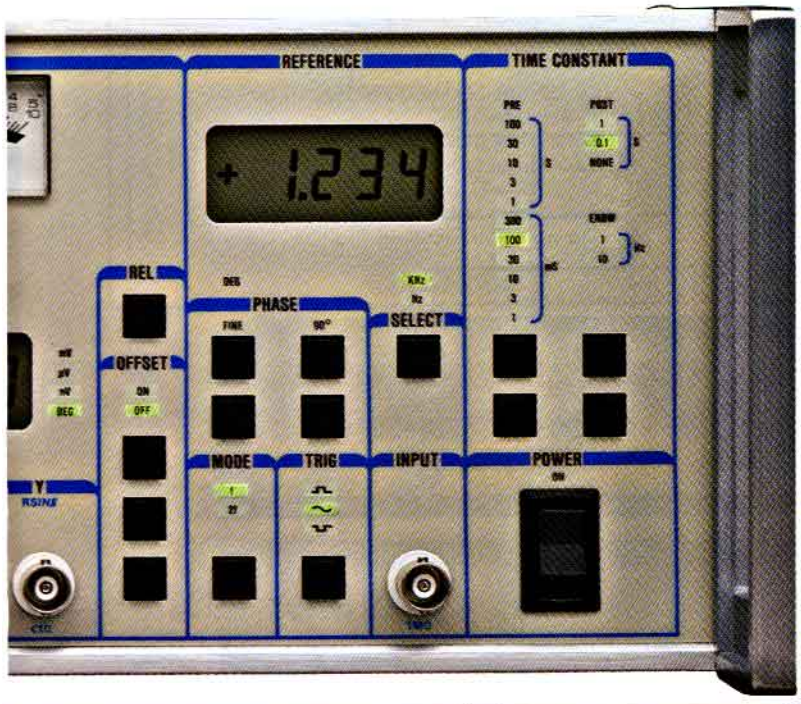
Features and Performance

Signal Channel

Current and Differential Voltage Inputs
Low Noise: 7 nV/√Hz
High Sensitivity: 10 nV or 0.1 pA Full Scale
Tracking Bandpass and Line Notch Filters
Dynamic Reserve up to 80 dB
Signal Monitor Output

Reference Channel

Wide Frequency Range: 1 Hz to 100 kHz
No Frequency Cards Required
Accurate, High Resolution Phase Control
Auto Phase (SR530)
Separate 1 Hz to 100 kHz Internal Oscillator
Internal Frequency Counter
May be Locked to f or 2f



Output Processing

Phase and Magnitude Measurement (SR530)
Time Constants from 1 mS to 100 S
Time Constants to 20 μS for Servo Systems
Excellent Harmonic Rejection
Analog and Digital Displays
Digital Frequency and Phase Display
Noise and Ratio Measurement
Stability Down to 5 ppm/°C

Computer Interface

RS-232 and IEEE-488
All Instrument Functions May Be Set
Four General Purpose A/D Inputs
Two General Purpose D/A Outputs

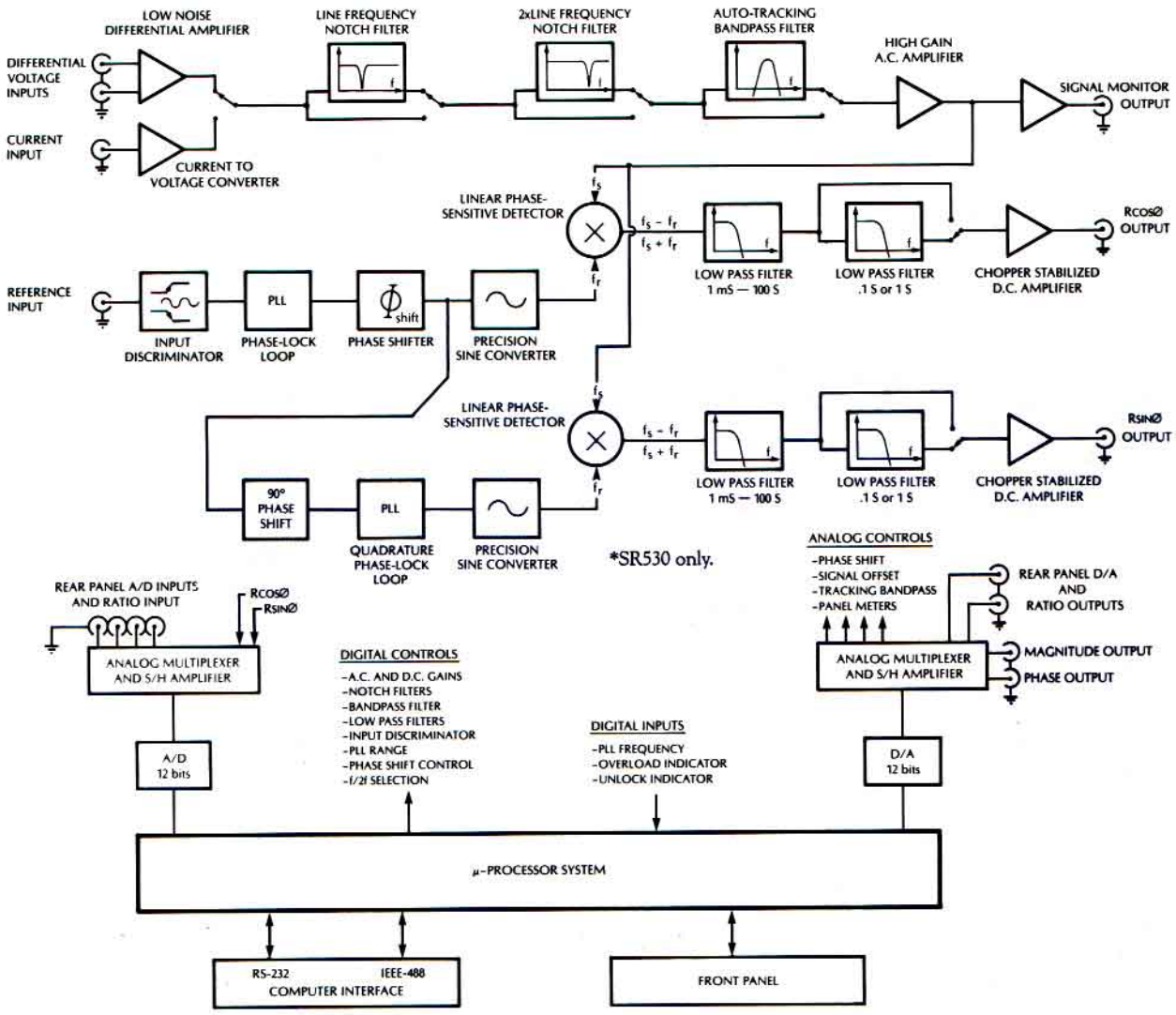
COMPUTER CONTROL

The internal microprocessor makes computer control of the lock-in easy. Both RS-232 and IEEE-488 interfaces are available and all instrument functions are controllable. Communication is simple: for example, you can read the frequency from the built-in frequency counter by sending the letter "F" or set the lock-in phase to 32.6 degrees by sending "P32.6." In addition, the lock-in can serve as your computer's link with other lab equipment through its four general purpose A/D inputs and two programmable D/A outputs.

PACKED WITH FEATURES

The SRS lock-ins are designed with extra features to help you solve your measurement problems. The internal oscillator operates from 1 Hz to 100 kHz and provides both a reference output and a signal output. The ratio feature can be used to normalize the signal to any source intensity fluctuations. The Expand and REL (Auto Offset) features allow you to instantly detect deviations from a baseline level up to ten times full scale. The RMS noise present in the signal can be measured over a 1 or 10 Hz equivalent bandwidth. And, the signal monitor provides an output port to view your ac amplified signal prior to demodulation.

STANFORD RESEARCH SYSTEMS
LOCK-IN AMPLIFIER BLOCK DIAGRAM



The Signal Channel

Each lock-in has both current and voltage inputs. The current input is a virtual ground, and the high impedance voltage inputs provide both signal-ended and true differential operation.

There are three signal filters. Each of these filters may be switched 'in' or 'out.' The first filter is a line notch filter. Set to either 50 or 60 Hz, this filter provides 50 dB of rejection at the line frequency. The second filter provides 50 dB of rejection at the second harmonic of the line frequency. The third filter is an auto-tracking bandpass filter with a center frequency tuned by the microprocessor to the frequency of the signal. These three filters eliminate most of the noise from the signal input before the signal is amplified.

A high-gain ac amplifier is used to amplify the signal before entering the phase-sensitive detector. The high gain which is available from this programmable amplifier allows the lock-in to operate with a lower gain in its dc amplifier. This arrangement provides high stability operation even when used on high sensitivity ranges.

Reference Channel and Phase-Sensitive Detector

The processor-controlled reference input discriminator can lock the instrument's PLL to a variety of reference signals. The PLL can lock to sine waves or to logic pulses with virtually no phase error. The PLL output is phase shifted and shaped to provide a precision sine wave to the phase sensitive detectors.

The phase-sensitive detector is a linear multiplier which mixes the amplified and filtered signal with the reference sine wave. The difference frequency component of the multiplier's output is a dc voltage proportional to the signal amplitude times the cosine of its phase. The SR530 two-phase lock-in has a second PSD to measure the signal amplitude times the sine of its phase which allows vector phase and magnitude calculations. The low-pass filters which follow the PSDs can reject signals which are more than a fraction of a Hertz away from the signal frequency.

A dc amplifier amplifies the output of the low-pass filters. The total system gain is the product of the ac and dc amplifier gains. The partitioning of the system gain between these two amplifiers will affect the stability and dynamic reserve of the instrument. The output is most stable when most of the gain is in the ac amplifier, however, high ac gain reduces the dynamic reserve.

For the most demanding applications the user may specify how the system gain is partitioned. However, with prefilters that are able to provide up to 100 dB of dynamic reserve, and with chopper stabilized dc amplifiers, most users will not be concerned with just how the system gain is allocated.

Microprocessor System

A Z-80-based microprocessor system is used to coordinate the instrument's functions. The processor updates displays, handles requests from the front panel, responds to interface commands, and controls the lock-in's gain, filter, and phase settings. The processor also updates analog outputs, does A/D conversions, measures frequency and computes ratios, phase angles, vector magnitudes, and noise values.

SR510 & SR530 Specification Summary

Signal Channel

Inputs	Voltage:	Single-ended or True Differential
	Current:	10* Volts/Amp
Full Scale Sensitivity	Voltage:	100 nV (10 nV on expand) to 500 mV
	Current:	100 fA to 0.5 μA
Impedance	Voltage:	100 MΩ+25 pF, ac coupled
	Current:	1 kΩ to virtual ground
Maximum Inputs	Voltage:	100 Vdc, 10 Vac damage threshold 2 Vac peak-to-peak saturation
	Current:	10 mA damage threshold 1 μA ac peak-to-peak saturation
Noise	Voltage:	7 nV/√Hz at 1 kHz
	Current:	0.13 pA/√Hz at 1 kHz
Common Mode	Range:	1 Volt peak; Rejection: 100 dB dc to 1 kHz Above 1 kHz the CMRR degrades by 6 dB/Octave
Gain Accuracy	1% (2 Hz to 100 kHz)	
Gain Stability	200 ppm/°C	
Signal Filters	60 Hz notch, −50 dB (Q=10 adjustable from 45 to 65 Hz) 120 Hz notch, −50 dB (Q=10 adjustable from 100 to 130 Hz) Tracking bandpass set to within 1% of ref freq (Q=5)	
Dynamic Reserve	20 dB LOW (1 μV to 500 mV sensitivity) 40 dB NORM (100 nV to 50 mV sensitivity) 60 dB HIGH (100 nV to 5 mV sensitivity) 80 dB with bandpass filter in Line Notch filters increase dynamic reserve to 100 dB	

Reference Channel

Frequency	1 Hz to 100 kHz
Input Impedance	1 MΩ, ac coupled
Trigger	SINE: 100 mV minimum, 1 Vrms nominal PULSE: ±1 Volt, 1 μsec minimum width
Mode	Fundamental (f) or 2nd Harmonic (2f)
Acquisition Time	25 Sec at 1 Hz 6 Sec at 10 Hz 2 Sec at 10 kHz
Phase Control	90° shifts Fine shifts in 0.025° steps
Phase Noise	0.01° rms at 1 kHz, 100 msec, 12 dB TC
Phase Drift	0.1°/°C
Phase Error	Less than 1° above 10 Hz
Orthogonality*	90° ±1°

Demodulator

Stability	5 ppm/°C on LOW dynamic reserve 50 ppm/°C on NORM dynamic reserve 500 ppm/°C on HIGH dynamic reserve
Time Constants	Pre: 1 msec to 100 sec (6 dB/Octave) Post: 1 sec, 0.1 sec, none (6 dB/Octave)
Offset	Up to 1× full scale (10× on expand) Both channels on the SR530 may be offset and expanded
Harmonic Rej	−55 dB (bandpass filter in)

Outputs & Interfaces

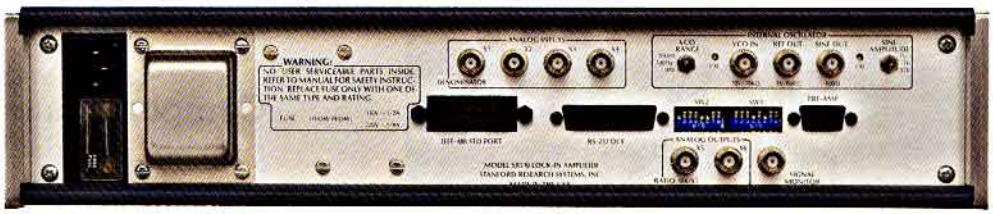
Channel 1 Outputs	X (RcosØ), X Offset, R (magnitude)*, R Offset*, X Noise, X5 (external D/A)*
Channel 2 Outputs*	Y (RsinØ), Y Offset, Ø (phase shift of signal), Y Noise, X6 (external D/A)
Output Meters	2% Precision mirrored analog meter
Output LCDs	Four digit auto-ranging LCD display shows same values as the analog meters
Output BNCs	±10 V output corresponds to full scale input <1 Ω output impedance
X Output*	X (RcosØ), ±10 V full scale, <1 Ω output impedance
Y Output*	Y (RsinØ), ±10 V full scale, <1 Ω output impedance
Reference LCD	Four digit LCD display for reference phase shift or frequency
RS-232	Interface controls all functions. Baud rates from 300 to 19.2 K
GPIB	Interface controls all functions. (IEEE-488 Std)
A/D	4 BNC inputs with 13 bit resolution (±10.24 V)
D/A	2 BNC outputs with 13 bit resolution (±10.24 V)
Ratio	Ratio output equals 10× Channel 1 output divided by the Denominator input.
Internal Oscillator	Range: 1 Hz to 100 kHz, 1% accuracy (100 Hz/V, 1 kHz/V, 10 kHz/V) Stability: 150 ppm/°C Distortion: 2% THD Amplitude: 1% accuracy, 500 ppm/°C stability 10 mV, 100 mV, 1 V RMS

General

Power	100, 120, 220, 240 Vac (50/60 Hz); 35 Watts Max
Mechanical	SR510: 17" x 17" x 3.5" (Rack Mount Included) 12 lbs SR530: 17" x 17" x 5.25" (Rack Mount Included) 16 lbs
Warranty	Two years parts and labor.

*SR530 only.

SR510
REAR PANEL



SR530
REAR PANEL

Specifications subject to change (01/03)

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